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Claim Amendments

Please amend claims 1 and 17 as follows.

Please cancel claims 8-16.

Please add new claims 21-23.

1. (currently amended) A semiconductor device hardmask ~~where during for~~ fabrication ~~[[the]]~~ of a semiconductor device compris[es]]ing:

a primary layer having for forming a feature having a first critical dimension specification;

a lower layer over the primary layer, the lower layer and the upper layer comprising a hardmask, the lower layer further having the first critical dimension subsequently hard-mask trimmed to satisfy the critical dimension specification of the primary layer etched in an isotropic etching step from a second critical dimension larger than the first critical dimension;

an upper layer over the lower layer, the upper layer having the second critical dimension formed from a first etching step and having a high-etching selectivity in the isotropic etching step as compared to the lower layer, ~~the upper layer substantially preventing thickness loss of the lower layer during hard-mask trimming, the lower layer and the upper layer have a substantially identical width wherein dimension after etching p, resulting from the lower layer and the upper layer being initially hard-mask etched together as a single hard-mask layer~~

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~~prior to hard mask trimming of the lower layer; and,~~

an etching-stop layer between the lower layer and the primary layer on which the first etching stop stops for ~~when hard mask etching of both the lower layer and the upper layer together as the single hard mask layer occurs.~~

2. (cancelled)

3. (original) The semiconductor device of claim 1, wherein the primary layer comprises one of a silicon layer and a polysilicon layer.

4. (original) The semiconductor device of claim 1, wherein the lower layer comprises a dielectric film.

5. (original) The semiconductor device of claim 1, wherein the upper layer comprises a dielectric film.

6. (original) The semiconductor device of claim 1, wherein the lower layer is selected from a group essentially consisting of: Si_3N_4 , SiON , and SiO_2 .

7. (original) The semiconductor device of claim 1, wherein the upper layer is selected from a group essentially consisting of: polysilicon, Si_3N_4 , SiON , and SiO_2 .

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8. - 16. (cancelled)

17. (currently amended) A semiconductor device that during fabrication is formed at least in part by a method comprising:

patterning a photoresist layer of a semiconductor wafer also having an upper layer under the photoresist layer and over a lower layer, said upper and lower layer comprising a hardmask;
[[and]]

a primary layer under the lower layer, the primary layer having a first critical dimension specification; the upper layer having a high-etching selectivity as compared to the lower layer in an isotropic etching step;

hard mask etching the lower layer and the upper layer together as a ~~single hard mask layer~~ down to an etching-stop layer between the lower layer and the primary layer, such that the lower layer and the upper layer have a ~~substantially identical width~~ second critical dimension after hard mask etching;

removing the photoresist layer;

hard mask trimming at least the lower layer from the second critical dimension; ~~the lower layer hard mask trimmed to satisfy the first critical dimension less than the second critical dimension specification of the primary layer,~~ the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming;

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removing the upper layer; and,
performing one or more actions selected from the group
essentially consisting of:

etching the primary layer for shallow trench isolation;
and,

etching the primary layer for gate formation and
removing the lower layer.

18. (cancelled)

19. (original) The semiconductor device of claim 17, wherein
each of the lower layer and the upper layer comprises a
dielectric film.

20. (original) The semiconductor device of claim 17, wherein
each of the lower layer and the upper layer is selected from a
group essentially consisting of: Si_3N_4 , SiON , and SiO_2 .

21. (new) The method of claim 1, wherein the isotropic etching
step is selected from the group consisting of a wet etching
process and a dry etching process.

22. (new) The method of claim 17, wherein the isotropic etching
step is selected from the group consisting of a wet etching
process and a dry etching process.

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23. (new) A method for forming a hardmask for etching a semiconductor device feature comprising the steps of:

patterning a photoresist layer over a hardmask layer comprising an upper and lower layer, said lower layer formed on an etching stop layer, said etching stop layer on a semiconductor layer;

etching through a thickness of the upper layer and lower layer to stop on the etching stop layer to form a first critical dimension;

removing the photoresist layer;

selectively etching the lower layer to form a second critical dimension less than the first critical dimension;

removing the upper layer; and,

etching the semiconductor feature through a thickness of the semiconductor layer according to the lower layer second critical dimension.